Fig. 1

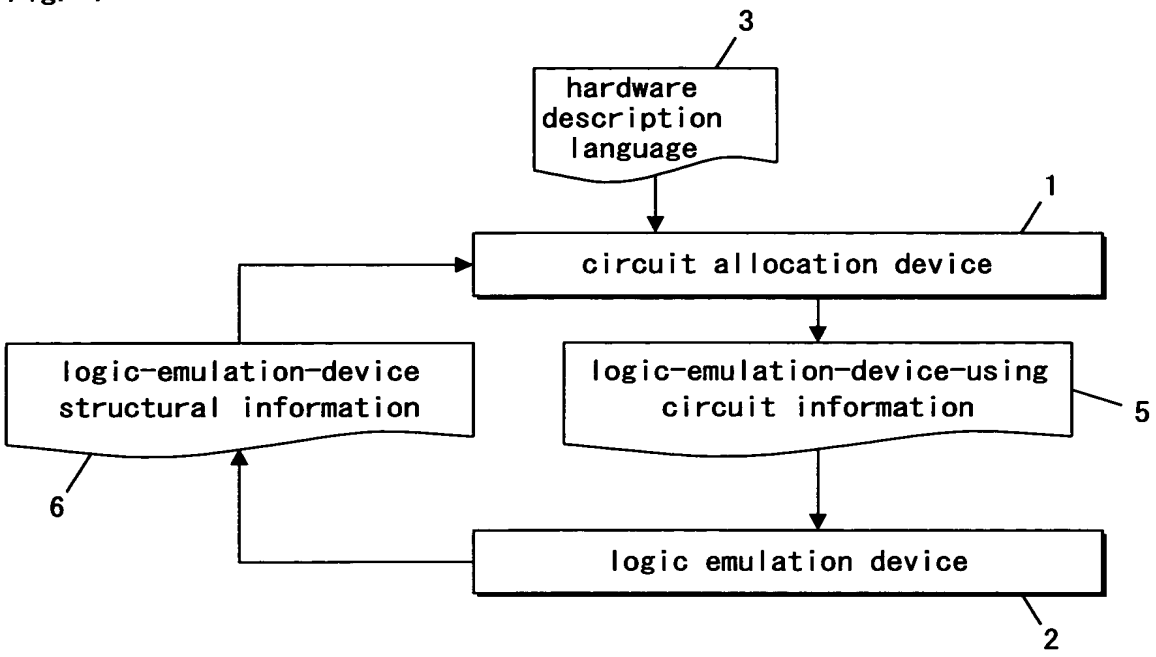

3
hardware description language
1
circuit allocation device
logic-emulation-device structural information
logic-emulation-device-using circuit information
5
6
logic emulation device
2

Fig. 2

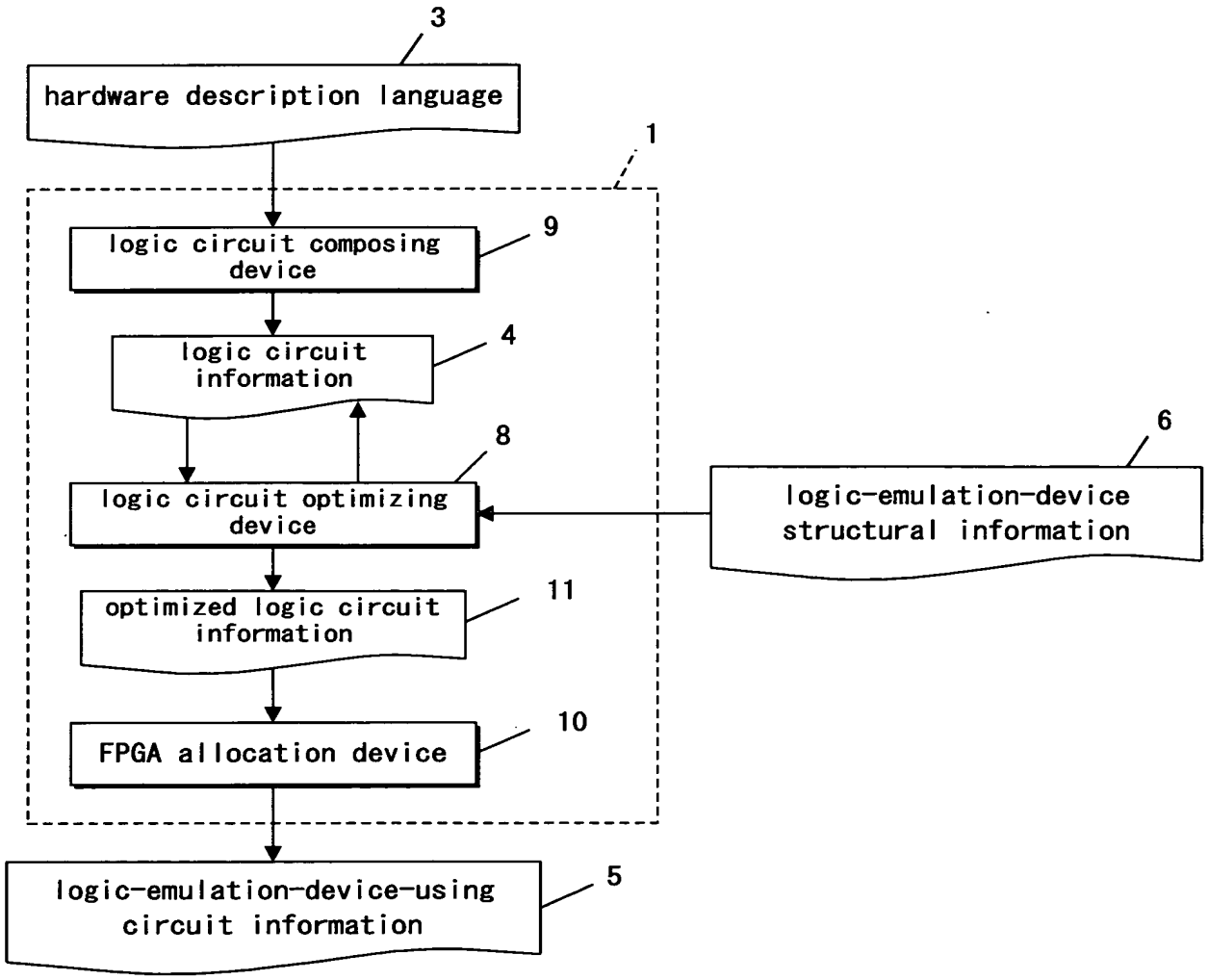

3
hardware description language
1
logic circuit composing device
9
logic circuit information
4
8
logic circuit optimizing device
6
logic-emulation-device structural information
optimized logic circuit information
11
FPGA allocation device
10
logic-emulation-device-using circuit information
5

Fig. 3

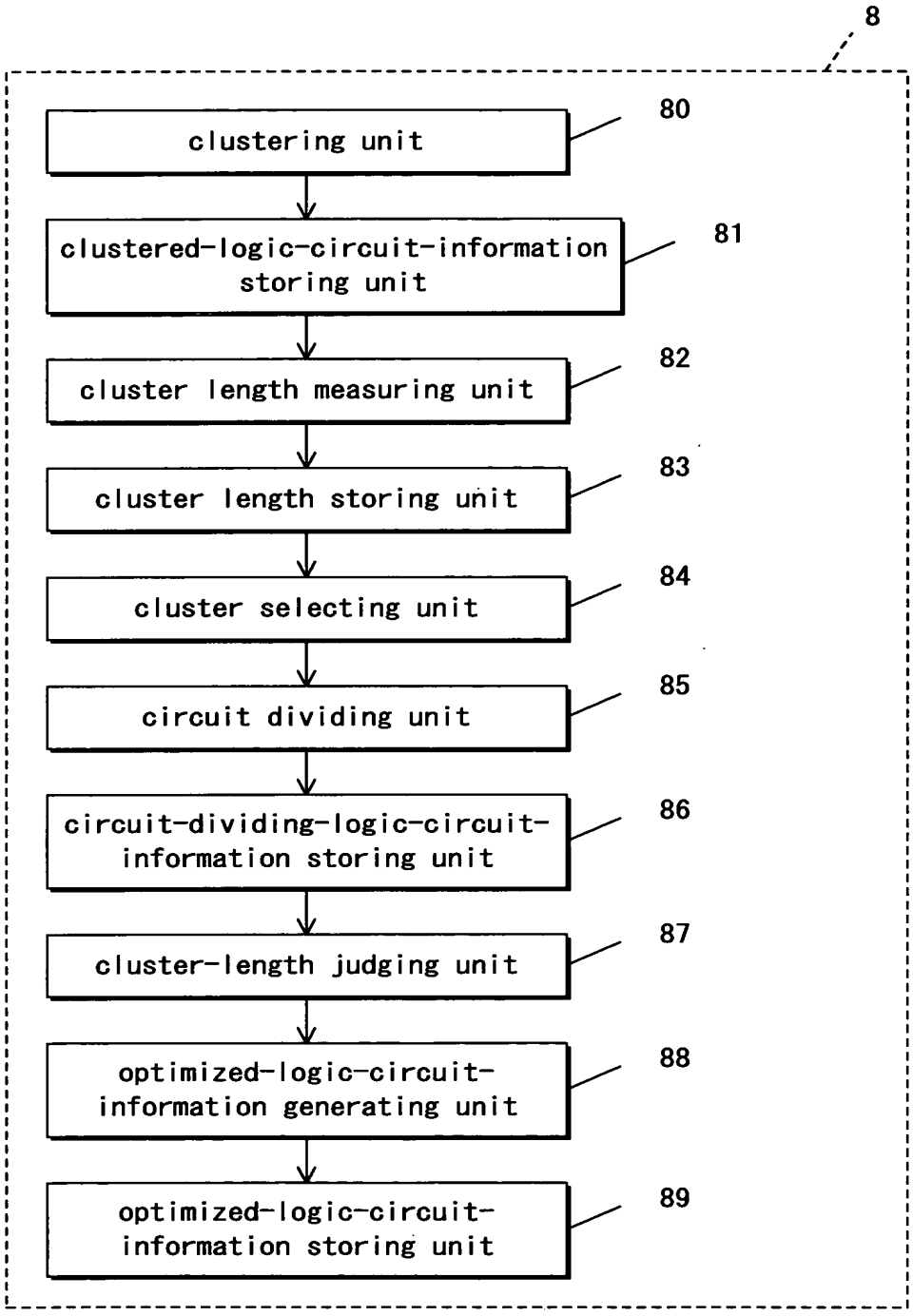

8
clustering unit
80
clustered-logic-circuit-information storing unit
81
cluster length measuring unit
82
cluster length storing unit
83
cluster selecting unit
84
circuit dividing unit
85
circuit-dividing-logic-circuit-information storing unit
86
cluster-length judging unit
87
optimized-logic-circuit-information generating unit
88
optimized-logic-circuit-information storing unit
89

Fig. 4(a)

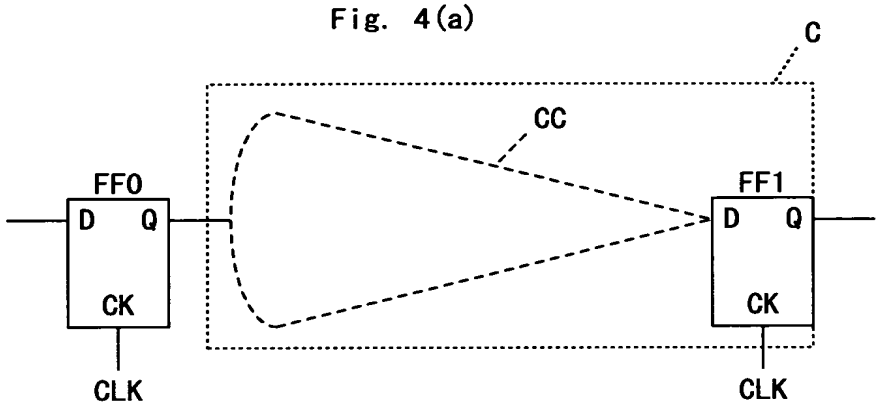

C
CC
FF0
D Q
CK
CLK
FF1
D Q
CK
CLK

Fig. 4(b)

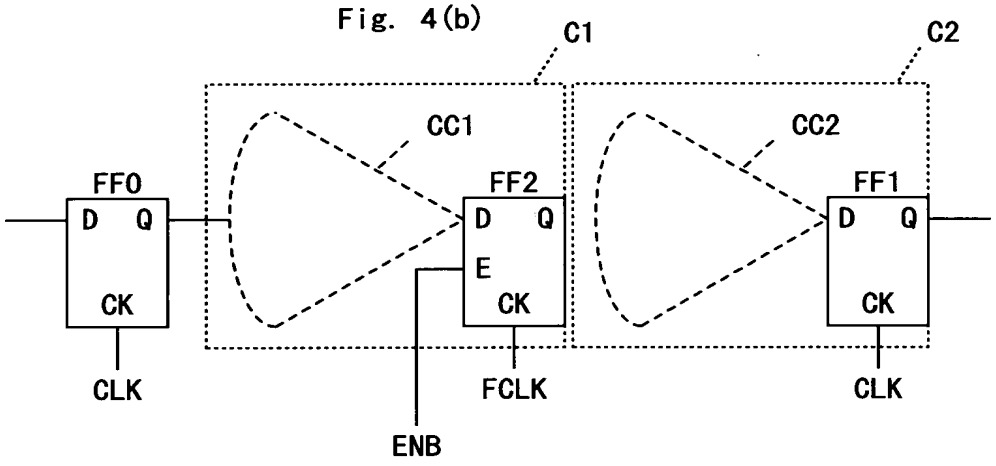

C1
C2
CC1
CC2
FF0
D Q
CK
CLK
FF2
D Q
E
CK
FCLK
ENB
FF1
D Q
CK
CLK

Fig. 5

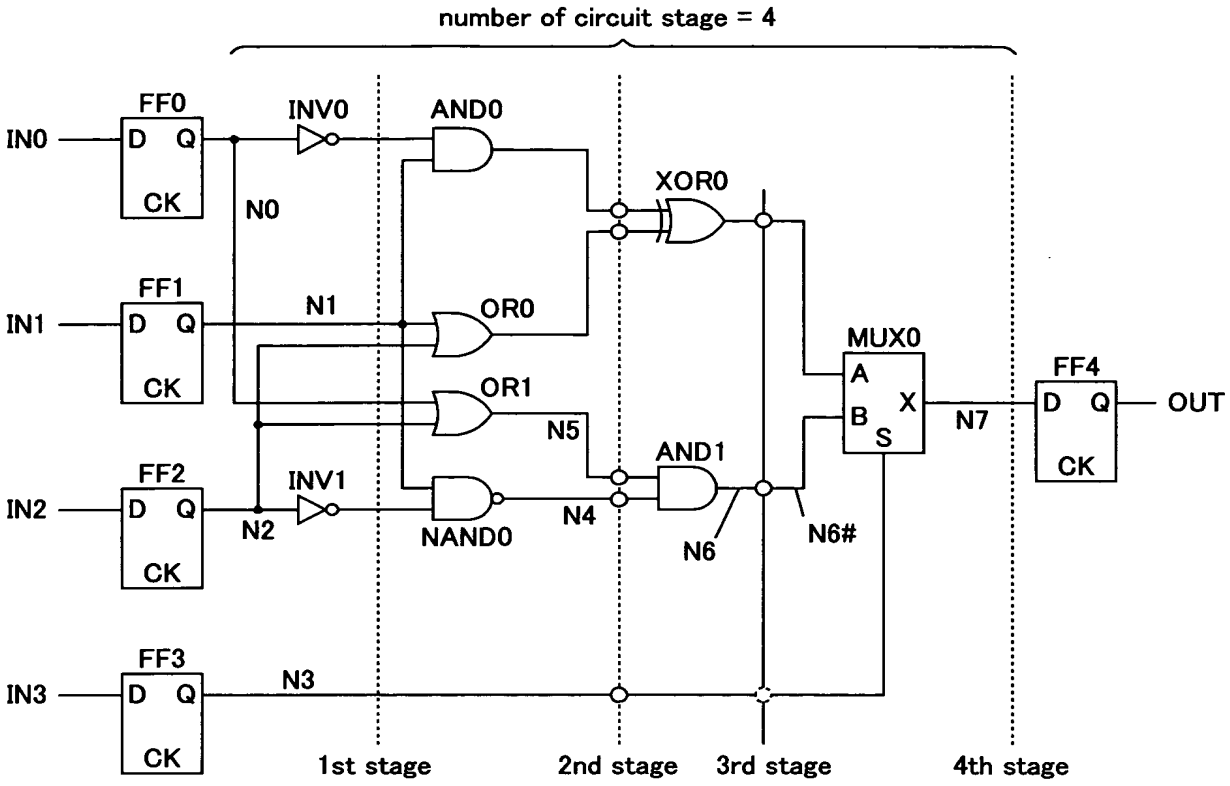

number of circuit stage = 4
IN0
IN1
IN2
IN3
FF0
FF1
FF2
FF3
D Q
CK
INV0
INV1
AND0
NAND0
OR0
OR1
XOR0
AND1
MUX0
A
B
X
S
FF4
OUT
N0
N1
N2
N3
N4
N5
N6
N6#
N7
1st stage
2nd stage
3rd stage
4th stage

Fig. 6

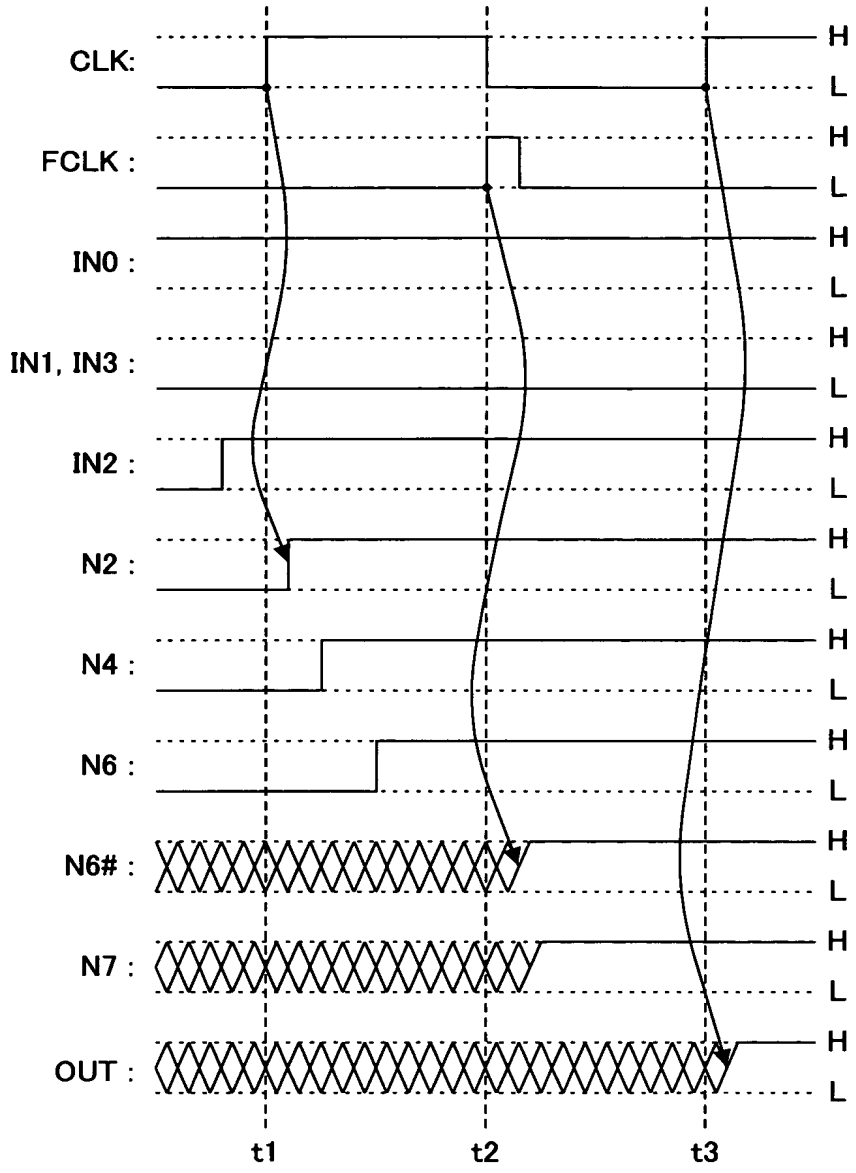


Fig. 7

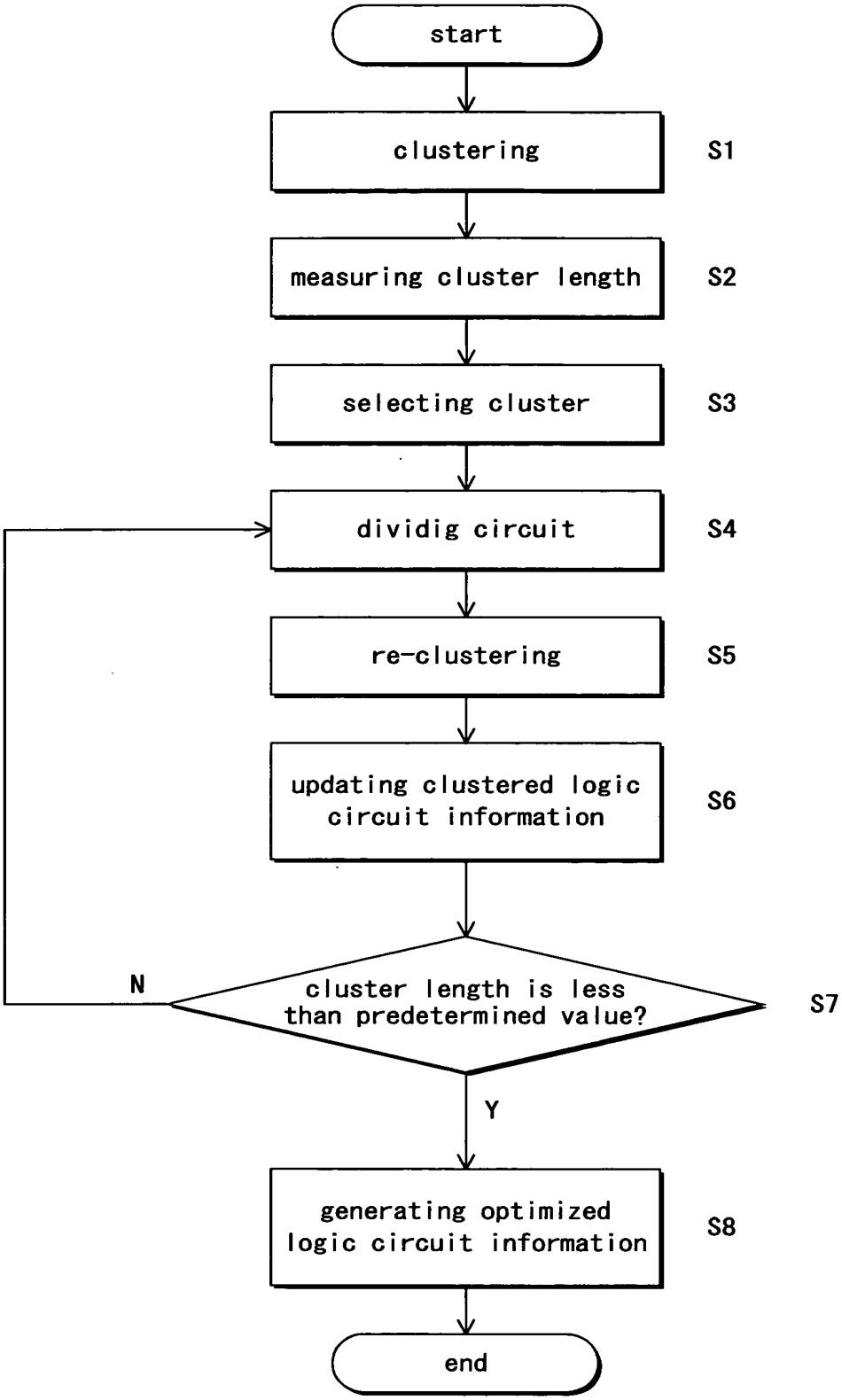
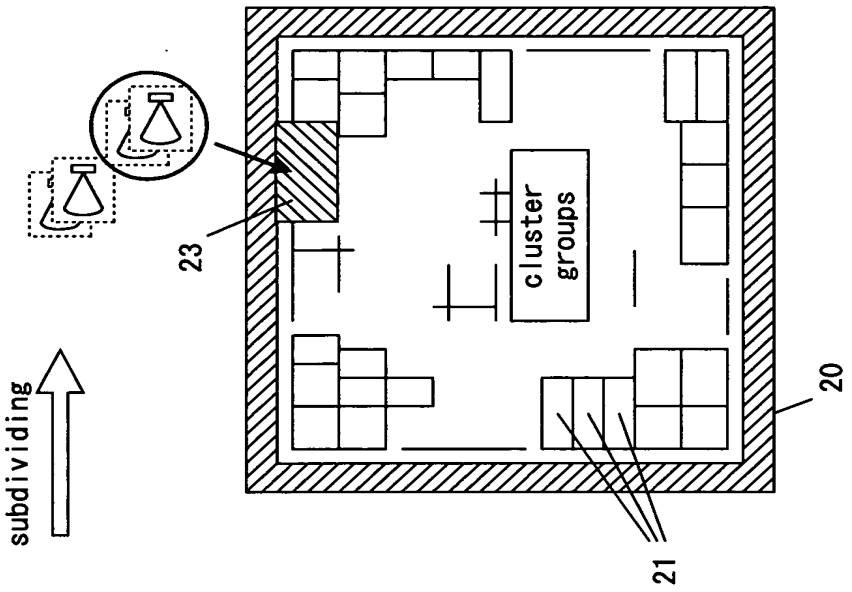

start
clustering
S1
measuring cluster length
S2
selecting cluster
S3
dividig circuit
S4
re-clustering
S5
updating clustered logic circuit information
S6
cluster length is less than predetermined value?
S7
N
Y
generating optimized logic circuit information
S8
end

Fig. 8(b)



subdividing

Fig. 8(a)

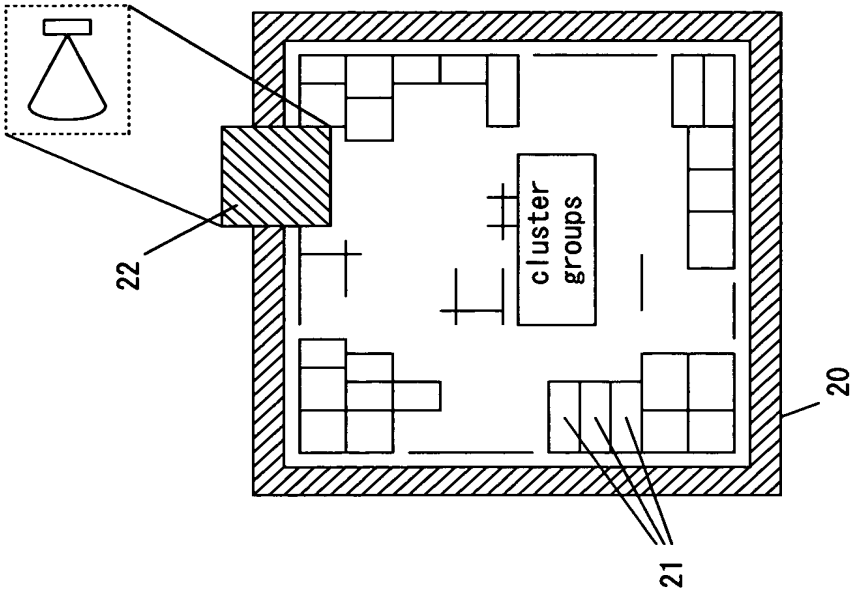


Fig. 9

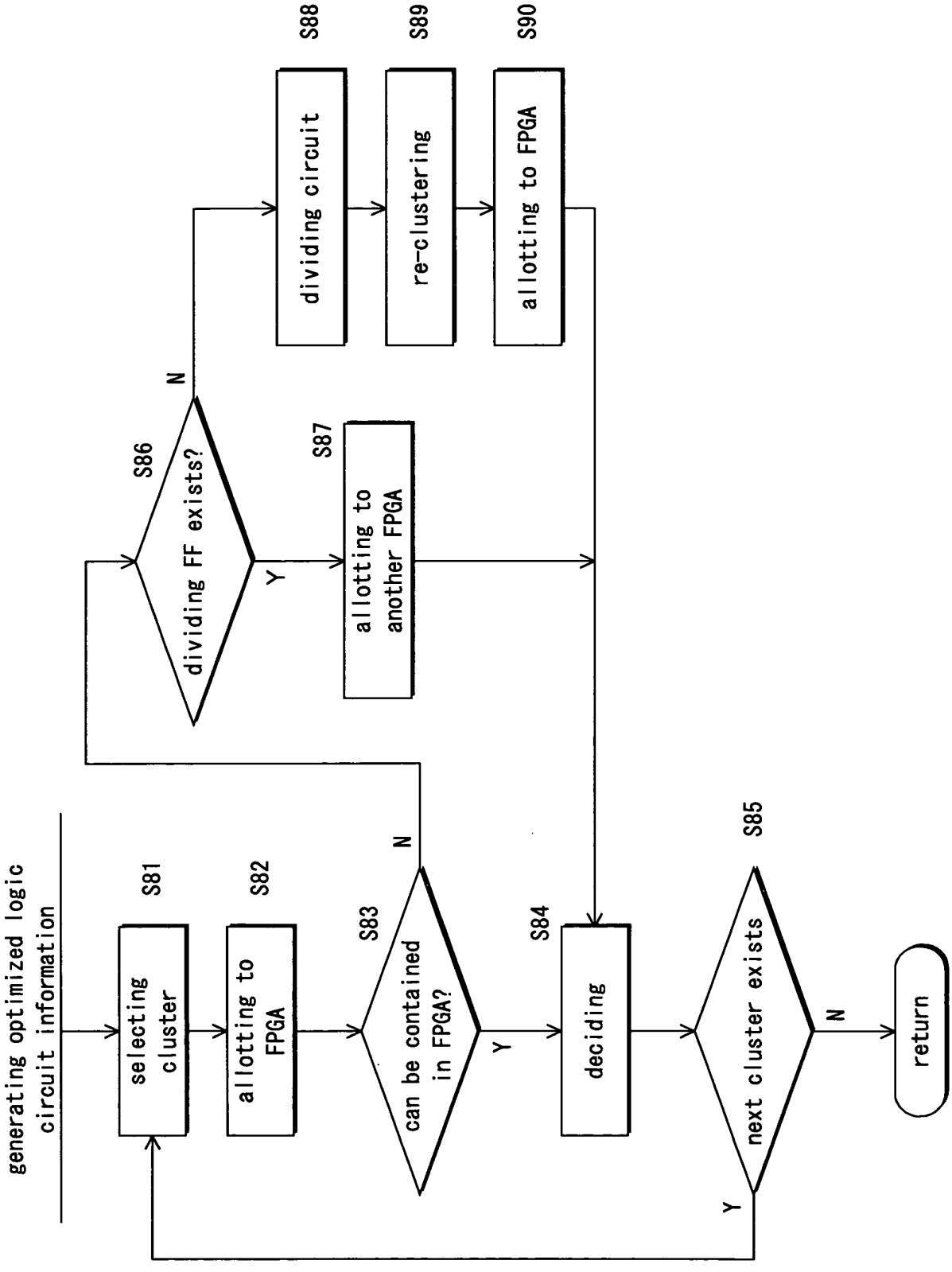

generating optimized logic circuit information
S81
selecting cluster
S82
allotting to FPGA
S83
can be contained in FPGA?
N
Y
S84
deciding
S85
next cluster exists
Y
N
return
S86
dividing FF exists?
N
Y
S87
allotting to another FPGA
S88
dividing circuit
S89
re-clustering
S90
allotting to FPGA

Fig. 10

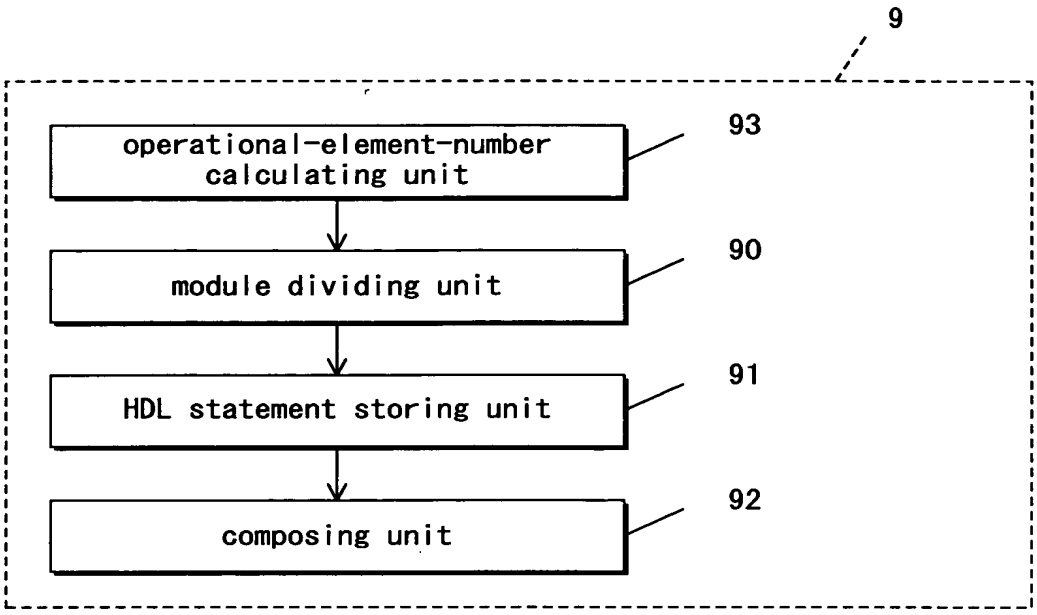


Fig. 11

```
module example_module(A,B,C,OUT)
input A,B,C;
output OUT;
x=(A+B)*(A*B);                    40
case OUT(C)                       41
    1'b0:OUT=x;
    1'b1:OUT= x;
endcase

endmodule
```

Fig. 12

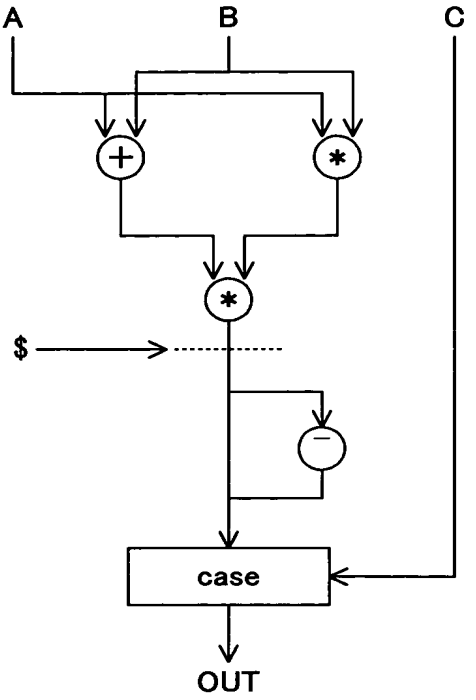


Fig. 13

```
module example_module(A,B,C,OUT)
input A,B,C;
output OUT;

x=(A+B)*(A*B);                          40

always(negedge CLK)                     42
    _x=x;

case OUT(C)                             41
      1'b0:OUT=_x;
      1'b1:OUT≅ _x;
endcase

endmodule
```

Fig. 14

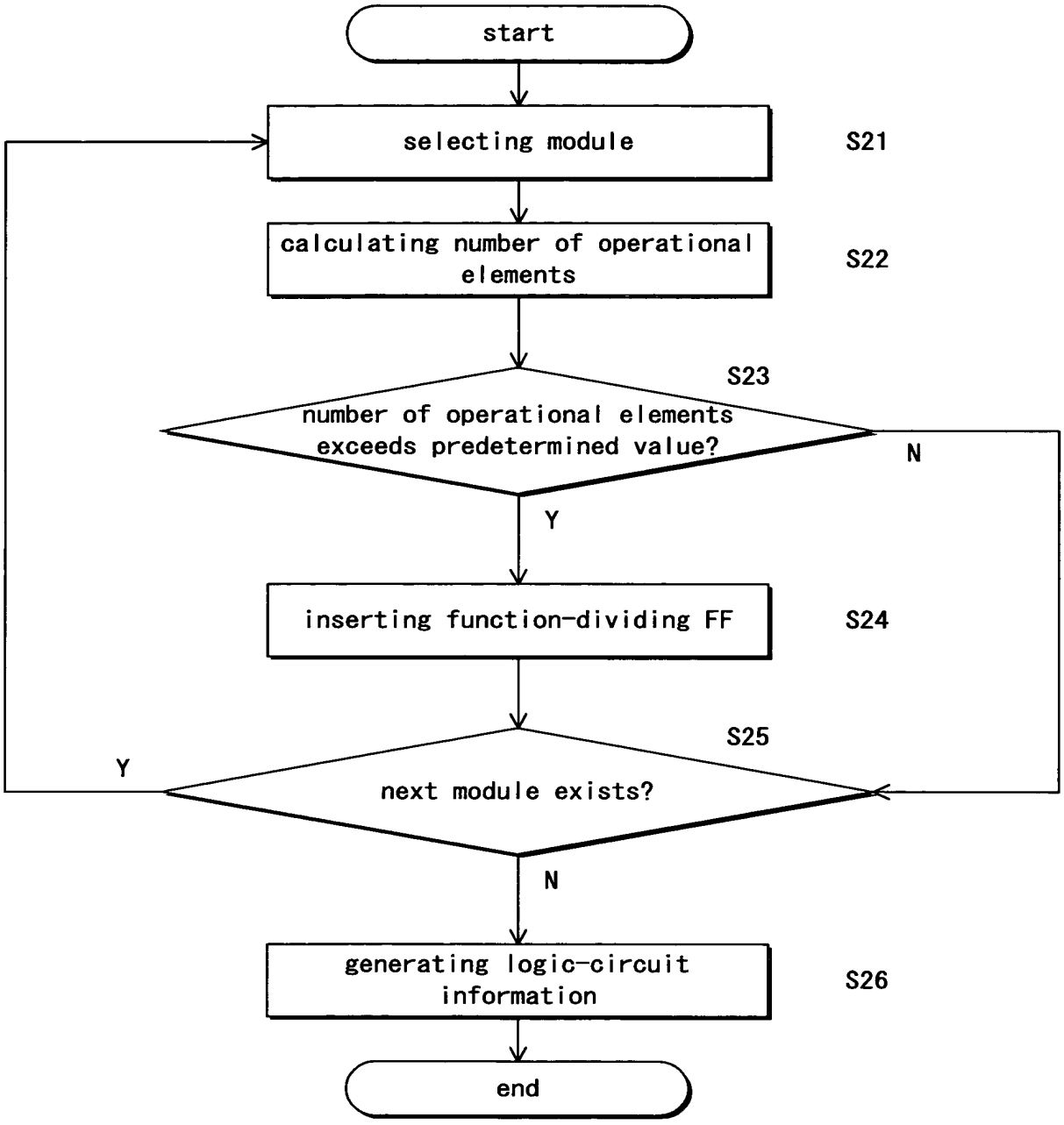

start
selecting module
S21
calculating number of operational elements
S22
S23
number of operational elements exceeds predetermined value?
N
Y
inserting function-dividing FF
S24
S25
Y
next module exists?
N
generating logic-circuit information
S26
end

Fig. 15

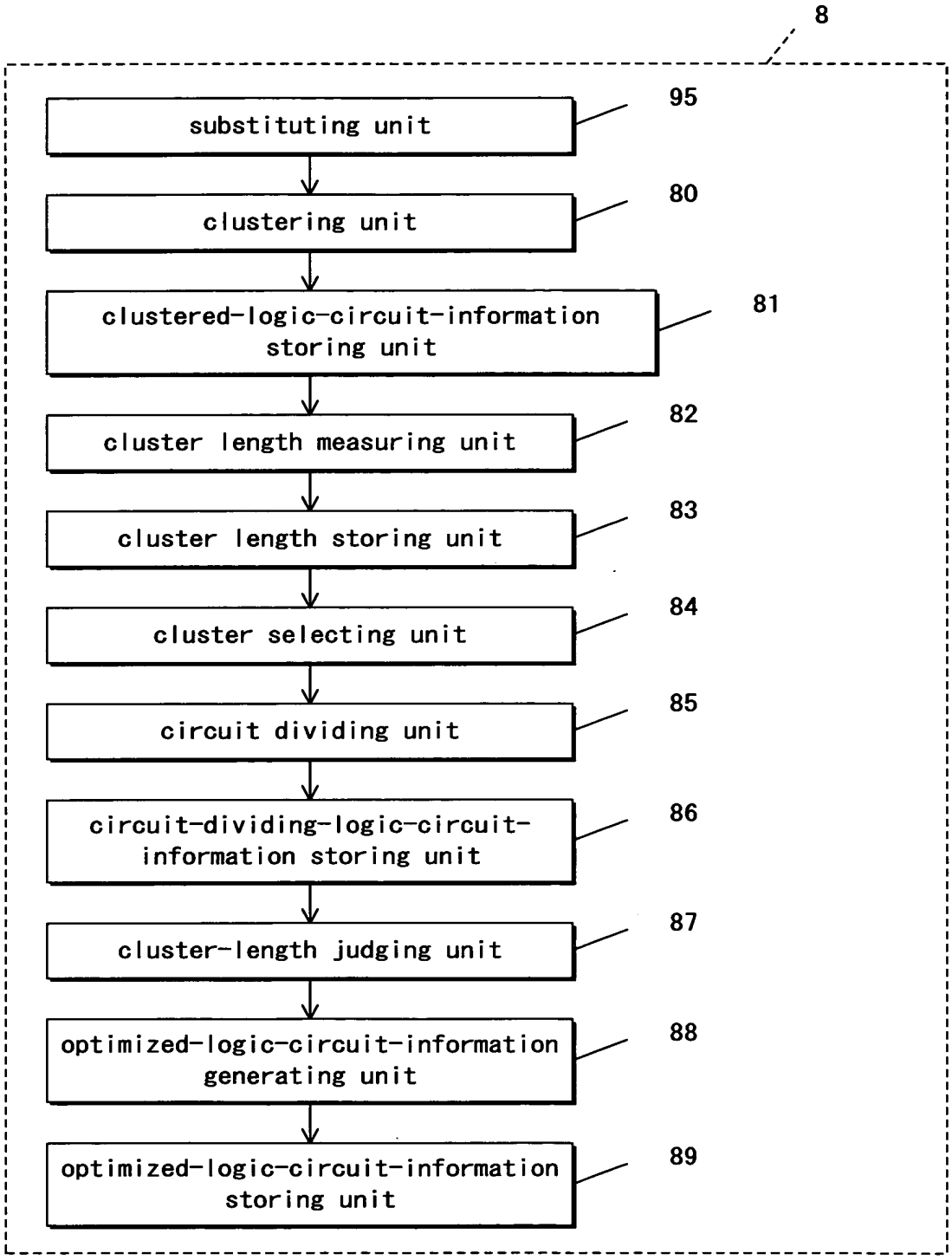

8
substituting unit
95
clustering unit
80
clustered-logic-circuit-information storing unit
81
cluster length measuring unit
82
cluster length storing unit
83
cluster selecting unit
84
circuit dividing unit
85
circuit-dividing-logic-circuit-information storing unit
86
cluster-length judging unit
87
optimized-logic-circuit-information generating unit
88
optimized-logic-circuit-information storing unit
89

Fig. 16

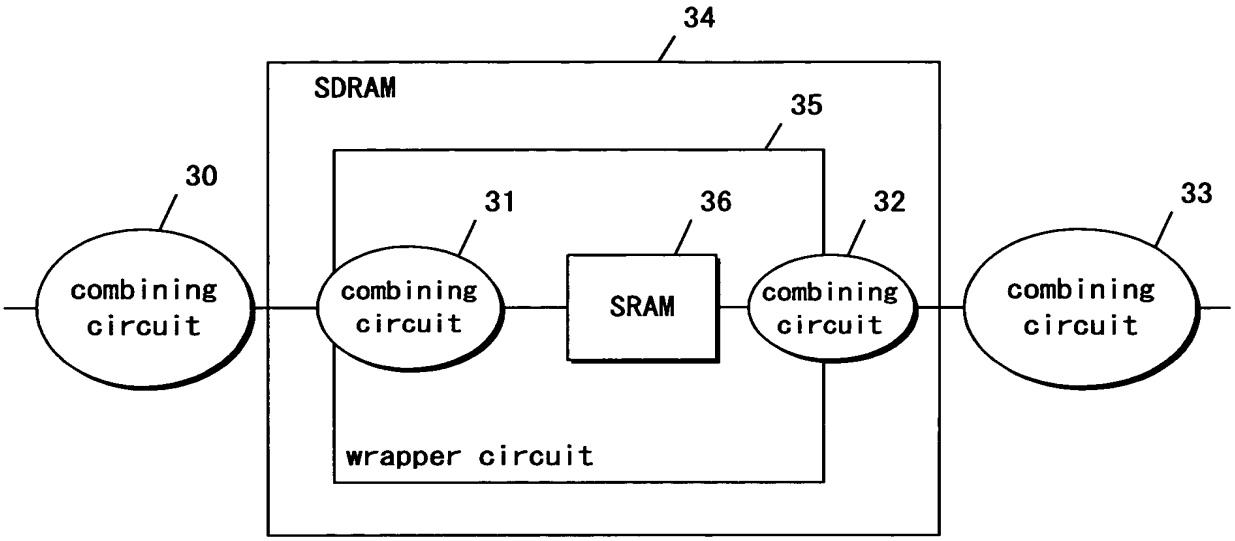


Fig. 17

kinds of memory	conversion value(number of circuit stages)
4Mbit SRAM	10
1Mbit SRAM	2

Fig. 18

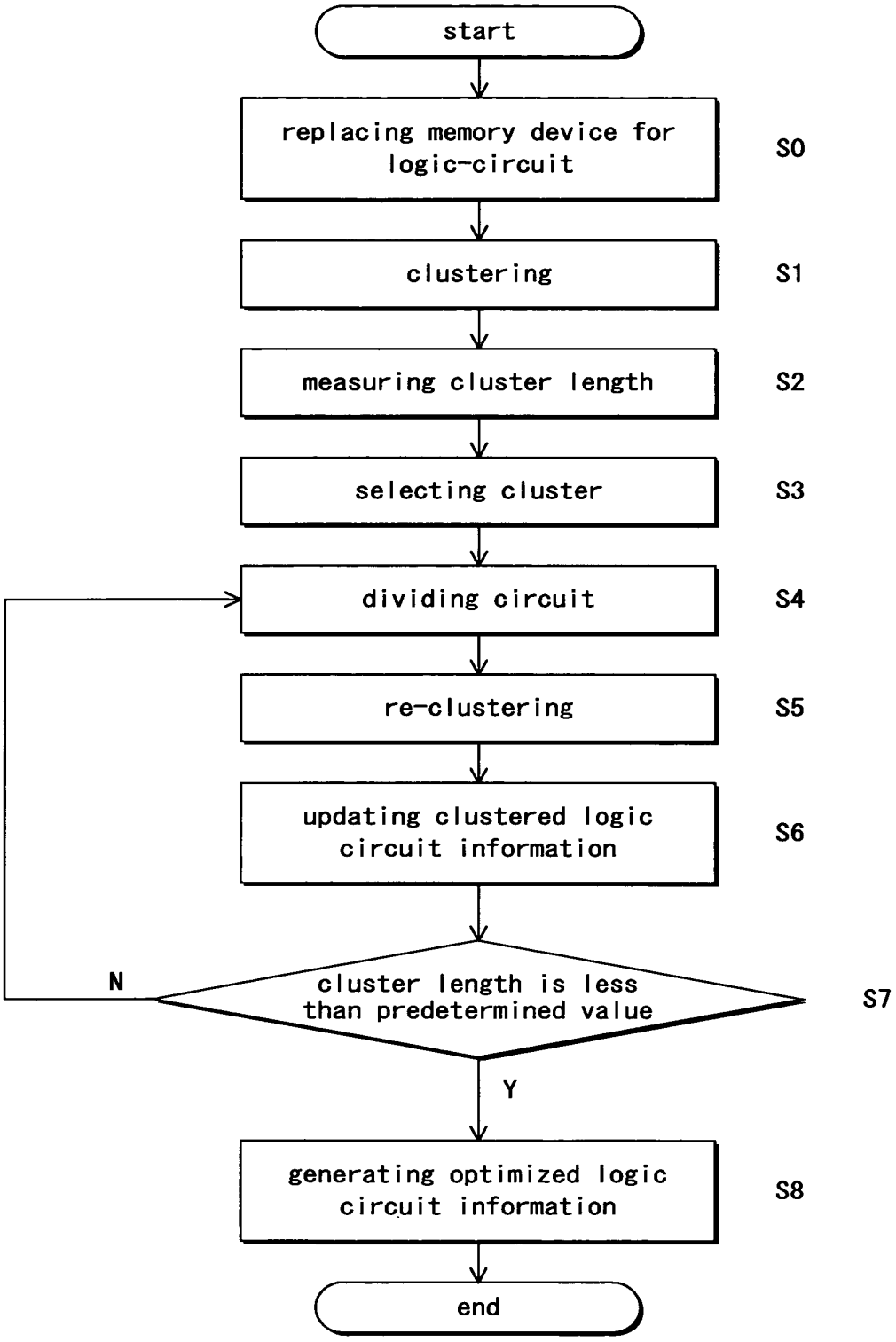

start
replacing memory device for logic-circuit
S0
clustering
S1
measuring cluster length
S2
selecting cluster
S3
dividing circuit
S4
re-clustering
S5
updating clustered logic circuit information
S6
cluster length is less than predetermined value
S7
N
Y
generating optimized logic circuit information
S8
end

Fig. 19

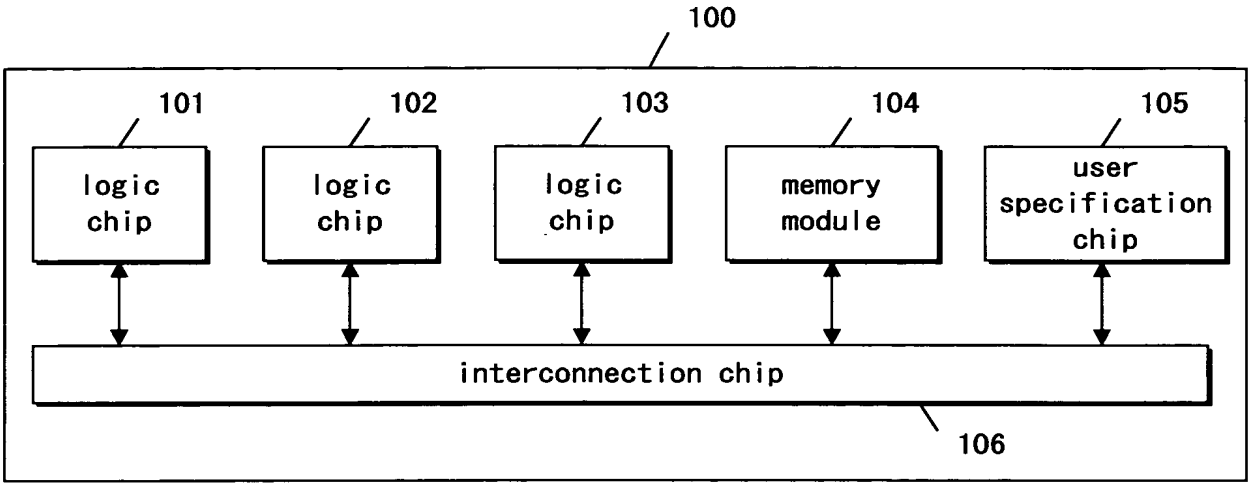

100
101
logic chip
102
logic chip
103
logic chip
104
memory module
105
user specification chip
interconnection chip
106

Fig. 20(a)

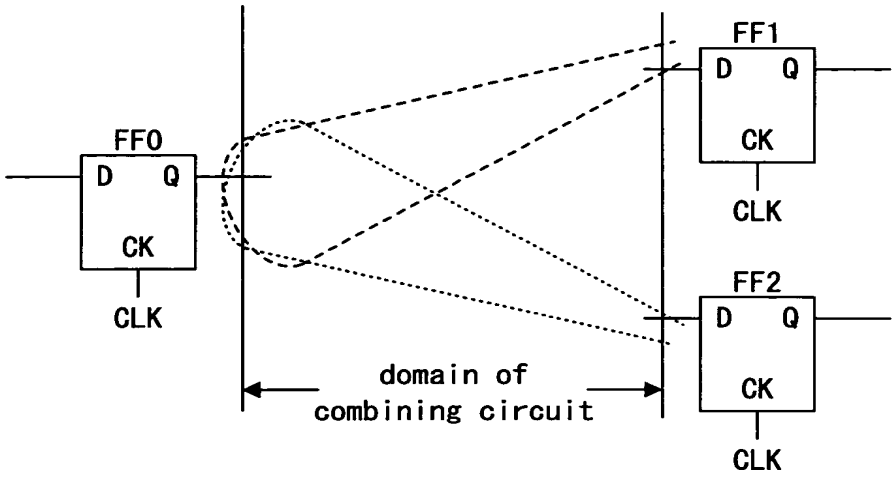


Fig. 20(b)

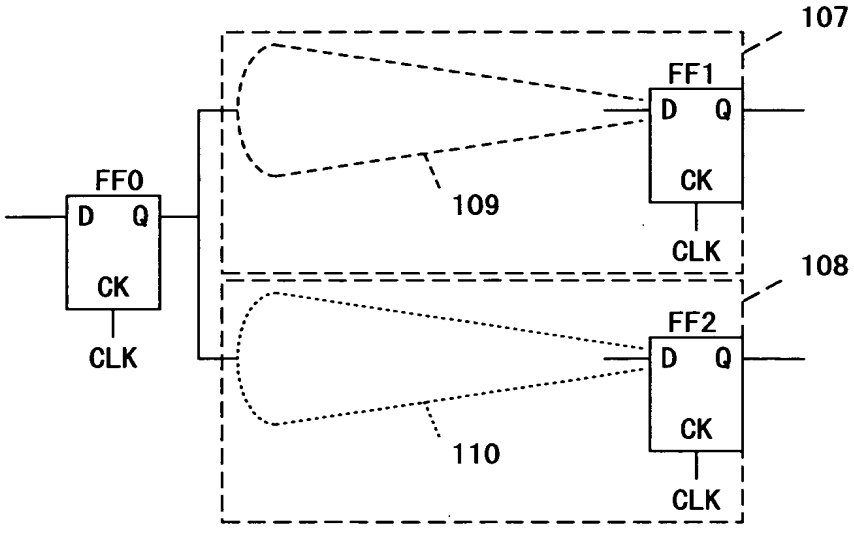


Fig. 21